UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,733	11/13/2003	Elmootazbellah Nabil Elnozahy	AUS920030760US1	2697

7590 04/13/2006

Jack V. Musgrove
2911 Briona Wood Lane
Cedar Park, TX 78613

EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 04/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,733	ELNOZAHY ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *21-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/13/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's election with traverse of claims 1-20 in the reply filed on March 20, 2006 is acknowledged. The traversal is on the ground(s) that claims 21-23 pertain to a computer memory system which allows access to virtual memory addresses that have changed based on a new memory mapping. This is not found persuasive because claims 1-20 disclose a method that allocates a new virtual address mapping using a memory controller to copy physical pages from old addresses to new addresses while claims 21-23 merely disclose cache that comprises a data array, tag array, cache controller, and state machine in which said cache stores cache status tag bits to maintain cache coherency. Thus, these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter.

The requirement is still deemed proper and is therefore made **FINAL**.

The instant application having Application No. 10/713,733 has a total of 23 claims pending in the application, there are 4 independent claims and 19 dependent claims. Claims 21-23 have been withdrawn from consideration and as such claims 1-20 are ready for examination by Examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration has been reviewed by Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

INFORMATION CONCERNING DRAWINGS

Drawings

2. Applicant's drawings submitted March 2, 2004 are acceptable for examination purposes.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

3. As required by MPEP § 609(c), Applicant's submission of the Information Disclosure Statement dated November 13, 2003 is acknowledged by Examiner and cited references have been considered in the examination of the claims now pending. As required by MPEP § 609 c(2), a copy of the PTOL-1449 initialed and dated by Examiner is attached to the instant office action.

OBJECTIONS

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is

suggested: "Superpage Coalescing Which Supports Read/Write Access To The New Virtual Superpage Mapping During Copying Of The Physical Pages."

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. **Claim 13** recites the limitation "said state machine" in line 2. There is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending the claim to read "said state engine."

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being obvious over Romer et al. "Reducing TLB and Memory Overhead Using Online Superpage Promotion", hereafter "Romer." in view of Arimilli et al. (U.S. Patent 6,907,494).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

10. **As per claim 1**, Romer discloses a method of assigning virtual memory to physical memory in a data processing system, comprising the steps of:

allocating a set of physical memory pages of the data processing system for a new virtual superpage mapping (pg. 178, section entitled "5 Mechanisms", lines 3-4 and 6-10);

instructing a memory controller of the data processing system to move a plurality of virtual memory pages corresponding to an old page mapping to the set of physical memory pages corresponding to the new virtual superpage mapping (pg. 178, section entitled "5 Mechanisms", lines 3-4 and 6-10). *It should be noted that Applicant's specification also indicates this limitation as admitted prior art on pg. 5, lines 16-17. It should also be noted that "processor" is analogous to "memory controller" and "copied" is analogous to "move."*

Romer does not expressly disclose accessing at least one of the virtual memory pages using the new virtual superpage mapping while the memory controller is copying old physical memory pages to new physical memory pages.

Arimilli discloses accessing at least one of the virtual memory pages using the new virtual superpage mapping while the memory controller is copying old physical memory pages to new physical memory pages (col. 8, lines 40-42; col. 9, lines 6-11). *It should be noted that "real address" is very similar to the "virtual address" used. The "real address" is simply the "virtual address" translated by the page translation table (col. 6, lines 22-29). The "real address" is then in turn mapped into a "physical address" by the memory controllers (col. 6, line 66 – col. 7, line 1).*

Romer and Arimilli are analogous art because they are from the same field of endeavor, that being virtual to physical page mapping.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Arimilli's memory controllers within Romer's superpage mapping system.

The motivation for doing so would have been because virtualization of physical memory occurs at the memory controller level of memory hierarchy, reconfigurations of multiple memory modules can be performed simultaneously while normal operations continue to operate on interconnect without special handling by the operating system or system processors (Arimilli, col. 11, lines 20-26).

Therefore, it would have been obvious to combine Romer and Arimilli for the benefit of obtaining the invention as specified in claim 1.

11. **As per claim 2**, Romer discloses said allocating step allocates a contiguous set of physical memory pages (pg. 178, section entitled "5 Mechanisms", lines 6-10).

12. **As per claim 3**, Arimilli discloses said accessing step includes the step of directing a read operation for an address of the new page mapping which is currently being copied to a corresponding address of an old page mapping (col. 8, lines 51-53).

13. **As per claim 4**, Arimilli discloses said accessing step includes the step of directing a write operation for an address of the new page mapping which is currently being copied to both the address of the new page mapping and a corresponding address of an old page mapping (col. 8, lines 53-58).

14. **As per claim 5**, Arimilli discloses said accessing step includes the step of directing a write operation for an address of the new page mapping which has not yet been copied to a corresponding address of an old page mapping (col. 8, lines 42-50). *It should be noted that "current" is analogous to "old."*

15. Claims 7, 9-15, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Armilli.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

16. **As per claim 7**, Arimilli discloses memory controller comprising:

an input for receiving page remapping instructions (Fig. 3, elements 325, 327, and 329).

a mapping table which temporarily stores entries of old page addresses and corresponding new page addresses associated with the page remapping instructions (col. 7, lines 58-65; Fig. 3, elements 301, 305, and 309); *It should be noted that "registers 301, 305, and 309" are analogous to a "mapping table", "current real address"*

is analogous to "old page address", and "new real address" is analogous to "new page address."

Arimilli also discloses a processing unit comprising a memory access device and a memory access device which directs the copying of memory pages from the old page addresses to the new page addresses and releases the entries in said mapping table as copying for each entry is completed (col. 7, lines 23-25; col. 8, line 66 – col. 9, line 4; Fig. 3, element 28).

Arimilli does not disclose a memory controller comprising a memory access device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate multiple move engines within each memory controller rather than having a singular move engine within the processing unit.

The motivation for doing so would have been to have move engines closer to registers 301, 305, and 309 (in which the move engines load addresses (col. 8, lines 9-10)) and also closer to the memory modules (in which the move engines transfer data (col. 7, lines 23-25), thus reducing data transfer latency and increasing overall system speed.

Therefore, it would have been obvious to Modify Arimilli for the benefit of obtaining the invention as specified in claim 7.

17. **As per claim 9**, Arimilli discloses said memory access device directs a read operation for a new page address which is currently being copied to a corresponding old page address (col. 8, lines 51-53).

18. **As per claim 10**, Arimilli discloses said memory access device directs a write operation for a new page address which is currently being copied to both the new page address and a corresponding old page address (col. 8, lines 53-58).

19. **As per claim 11**, Arimilli discloses said memory access device directs a write operation for a new page address which has not yet been copied to a corresponding old page address (col. 8, lines 42-50). *Please see citation note for claim 5 above.*

20. **As per claim 12**, Arimilli discloses said memory access device includes a state engine which sequentially reads the paired old and new pages addresses in said mapping table (col. 7, lines 25-28; col. 8, lines 51-58; Fig. 3, elements 26, 36, and 46). *It should be noted that "mapping engine" is analogous to "state engine."*

21. **As per claim 13**, Arimilli discloses said memory access device further includes a direct memory access (DMA) engine controlled by said state machine which carries out actual copying of the memory pages (col. 7, lines 23-25 and 58-65; col. 8, lines 9-10; Fig. 3, element 28). *It should be noted that "move engine" is analogous to "DMA engine." It should also be noted that it is the move engine use registers 301, 305, and 309 for the memory re-configuration and these registers are located on the mapping engine, thus, the mapping engine inherently controls the move engine.*

22. **As per claim 14**, Arimilli discloses a computer system comprising:

a processing unit (col. 4, lines 17-19; Fig. 3, element 10);

an interconnect bus connected to said processing unit (col. 4, lines 17-19, Fig. 3, element 12);

a memory array (col. 4, lines 29-32; Fig. 3, elements 22, M1, M2, and M3); *It should be noted that "physical memory (memory modules M1, M2, and M3)" is analogous to "memory array."*

and a memory controller connected to said interconnect bus and said memory array (col. 4, lines 40-42; Fig. 3, elements 24, 34, and 44),

wherein said memory controller copies memory pages from old page addresses to new page addresses while said processing unit carries out program instructions using the new page addresses (col. 7, lines 23-25; col. 4, lines 19-23). *Please see citation note for claim 7 above.*

23. **As per claim 15**, Arimilli discloses said processing unit includes a processor core having a translation lookaside buffer (TLB) whose entries keep track of current virtual-to-physical memory address assignments (col. 5, lines 43-46);

and said TLB entries are updated for the new page addresses prior to completion of copying of the memory pages by the memory controller (col. 9, lines 4-11). *It should be noted that for the system to use a "virtualized physical mapping" it is inherently required the TLB be updated with the new addresses because the TLB is the only mechanism capable of translating virtual into real addresses.*

24. **As per claim 19**, Arimilli discloses said memory controller includes:

a mapping table which temporarily stores entries of old page addresses and corresponding new page addresses (col. 7, lines 58-65; Fig. 3, elements 301, 305, and 309);

and a memory access device which directs the copying of the memory pages from the old page addresses to the new page addresses and releases the entries in said mapping table as copying for each entry is completed (col. 7, lines 23-25; col. 8, line 66 – col. 9, line 4; Fig. 3, element 28). *It should be noted that claim 19 stands rejected under the same grounds as the 35 USC 103 rejection of claim 7 above.*

25. **As per claim 20**, Arimilli discloses said processing unit, said interconnect bus, said memory array and said memory controller are all part of a first processing cluster, and further comprising a network interface which allows said first processing cluster to communicate with a second processing cluster, said memory controller having at least one pointer for a new page address which maps to a physical memory location in said second processing cluster (col. 5, lines 54-58; Fig. 3, element 8). *It should be noted that the "data processing system" is analogous to the "first cluster" and "port connection to networks" is analogous to "network interfaces."*

26. Claim 6 is rejected under 35 U.S.C. 103(a) as being obvious over Romer in view of Arimilli as applied to claim 1 above, and in further view of Belair (U.S. Patent 6,212,613).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject

matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

27. Romer/Arimilli discloses all of the limitations of claim 6 except the step of updating an entry in a cache memory of the data processing system which corresponds to a memory location in the virtual memory page, by modifying an address tag of the cache entry according to the new page mapping.

Belair discloses the step of updating an entry in a cache memory of the data processing system which corresponds to a memory location in the virtual memory page, by modifying an address tag of the cache entry according to the new page mapping (col. 6, lines 46-47; col. 9, lines 36-41; Fig. 1, element 22; Fig. 2, element 42).

Romer/Arimilli and Belair are analogous art because they are from the same field of endeavor, that being virtual to physical page mapping.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Belair's cache with corresponding TLB within Romer/Arimilli's processing unit.

The motivation for doing so would have been to have TLB maintenance operations involved in responding to a dynamic mapping request simpler and faster (Belair, col. 5, lines 46-48).

Therefore, it would have been obvious to combine Romer/Arimilli and Belair for the benefit of obtaining the invention as specified in claim 6.

28. Claim 8 is rejected under 35 U.S.C. 103(a) as being obvious over Arimilli in as applied to claim 7 above, and in further view of Romer.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

29. Arimilli discloses all the limitations of claim 8 except said mapping table has 32 slots for receiving corresponding pairs of the old page addresses and new page addresses.

Romer discloses said mapping table has 32 slots for receiving corresponding pairs of the old page addresses and new page addresses (pg. 178, italicized section entitled "Table 2", line 4). *It should be noted that "entries" is analogous to "slots."*

Arimilli and Romer are analogous art because they are from the same field of endeavor, that being virtual to physical page mapping.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Arimilli's registers (i.e. mapping table) as Romer's 32 TLB.

The motivation for doing so would have been to improve system performance by increasing instructions per TLB miss (Romer, pg. 187, section entitled "Capacity Counters", last paragraph).

Therefore, it would have been obvious to combine Arimilli and Romer for the benefit of obtaining the invention as specified in claim 8.

30. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being obvious over Arimilli as applied to claim 14 above, and in further view of Belair.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an

invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

31. **As per claim 16**, Arimilli discloses said processing unit has a processor core (col. 4, lines 20-22; Fig. 1, element 14).

Arimilli does not expressly disclose said processing unit has an associated cache;

and said cache modifies an address tag of a cache entry which corresponds to a memory location in the new page addresses.

Belair discloses disclose said processing unit has an associated cache (col. 6, lines 26-27; Fig.1, element 14 and 22);

and said cache modifies an address tag of a cache entry which corresponds to a memory location in the new page addresses (col. 6, lines 46-47; col. 9, lines 36-41; Fig. 1, element 22; Fig. 2, element 42).

Arimilli and Belair are analogous art because they are from the same field of endeavor, that being virtual to physical page mapping.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Belair's cache with corresponding TLB within Arimilli's processing unit.

The motivation for doing so would have been to have TLB maintenance operations involved in responding to a dynamic mapping request simpler and faster (Belair, col. 5, lines 46-48).

Therefore, it would have been obvious to combine Arimilli and Belair for the benefit of obtaining the invention as specified in claim 16.

32. **As per claim 17**, Arimilli discloses said cache modifies the address tag of the cache entry in response to a determination that the cache entry contains a valid value which is not present elsewhere in the system (col. 9, lines 43-45). *It should be noted that "entry 2" points to a distinct physical memory location (x8000), thus, entry 2's value is not present elsewhere in the system.*

33. **Claim 18 is rejected under 35 U.S.C. 103(a) as being obvious over Arimilli in further view of Belair as applied to claim 16 above, and in further view of Evans et al. (U.S. Patent 6,732,238).**

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject

matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

34. Arimilli/Belair discloses all the limitations of claim 18 except said cache further relocates the cache entry based on a changed congruence class for the modified address tag.

Evans discloses said cache further relocates the cache entry based on a changed congruence class for the modified address tag (col. 4, lines 27-34; col. 7, lines 48-64). *It should be noted that "replacement" is analogous to "relocate" and "associativities with different number of indices" is analogous to "different congruence classes."*

Arimilli/Belair and Evans are analogous art because they are from the same field of endeavor, that being updating TLB entries.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Evans's TLB replacement algorithm within Arimilli/Belair's TLB.

The motivation for doing so would have been an efficient and scalable implementation that provides good performance on the level of LRU, random, and clocked replacement algorithms (Evans, col. 4, lines 35-37).

Therefore, it would have been obvious to combine Arimilli/Belair and Evans for the benefit of obtaining the invention as specified in claim 18.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-20** have received a first action on the merits and are subject of a first action non-final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 5,784,707 discloses a method and apparatus for managing virtual computer memory with multiple page sizes.

2. U.S. Patent 5,835,964 discloses a virtual memory system with hardware TLB and unmapped software TLB updated from mapped task address maps using unmapped kernel address map.

3. U.S. Patent 6,073,226 discloses a system and method for minimizing page tables in virtual memory systems.

4. U.S. Patent 6,085,296 discloses sharing memory pages and page tables among computer processes.

5. U.S. Patent 6,434,681 discloses a snapshot facility for a data storage system permitting continued host read/write access.

6. U.S. Patent 6,904,490 discloses a method and system of managing virtualized physical memory in a multi-processor system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Arpan Savla
Assistant Examiner
Art Unit 2185
April 7, 2006

DONALD SPARKS
SUPERVISORY PATENT EXAMINER